

FEATURES

TL082/TL084 compatible

Low input bias current: 10 pA maximum

Offset voltage

5.5 mV maximum (ADTL082A/ADTL084A)

9 mV maximum (ADTL082J/ADTL084J)

±15 V operation

Low noise: 16 nV/√Hz

Wide bandwidth: 5 MHz

Slew rate: 20 V/μs

CMRR: 80 dB minimum

Total harmonic distortion: 0.001%

Supply current: 1.2 mA typical

Unity-gain stable

APPLICATIONS

General-purpose amplification

Power control and monitoring

Active filters

Industrial/process control

Data acquisition

Sample and hold circuits

Integrators

Input buffering

GENERAL DESCRIPTION

The ADTL082 and ADTL084 are JFET input amplifiers that provide industry-leading performance over TL08x devices. The ADTL082A and ADTL084A are improved versions of TL08x A, I, and Q grades. The ADTL082J and ADTL084J are industry alternatives to the TL08x standard and C grades.

The ADTL08x family offers lower noise, offset voltage, offset drift over temperature, and bias current over the TL08x. In addition, the ADTL08x family has better common-mode rejection and slew rates.

These op amps are ideal for various applications, including process control, industrial and instrumentation equipment,

active filtering, data conversion, buffering, and power control and monitoring.

The A grade amplifiers are available in lead-free packaging. The standard grade amplifiers are available in both leaded and lead-free packaging.

The ADTL082A and ADTL084A are specified over the extended industrial (−40°C to +125°C) temperature range. The ADTL082J and ADTL084J are specified over the commercial (0°C to 70°C) temperature range.

PIN CONFIGURATIONS



Figure 1. 8-Lead SOIC_N (R-8)

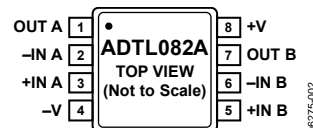


Figure 2. 8-Lead MSOP (RM-8)

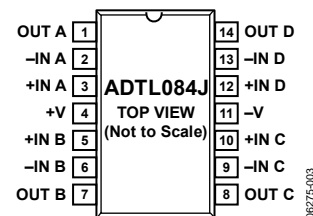


Figure 3. 14-Lead SOIC_N (R-14)

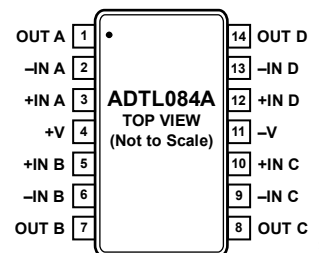


Figure 4. 14-Lead TSSOP (RU-14)

Rev. A

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REVISION HISTORY

4/07—Rev. 0 to Rev. A

Changes to Table 1	3
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1/07—Revision 0: Initial Version

SPECIFICATIONS

$V_{CC} = \pm 15\text{ V}$, $V_{CM} = 0\text{ V}$, $T_A = 25^\circ\text{C}$, over all grades, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	J Grade			A Grade			Unit
			Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS									
Offset Voltage	V_{OS}	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$		2	9		1.5	5.5	mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			10		8		mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$		15				9	$\mu\text{V}/^\circ\text{C}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$					10		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$		2	100		2	100	pA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			3			3	nA
Input Offset Current	I_{OS}	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$		2	100		2	100	pA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			3			3	nA
Input Voltage Range	V_{CM}		-11		+15	-11		+15	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -11\text{ V to }+15\text{ V}$	80	86		80	86		dB
Input Impedance	R_{IN}				10^{12}			10^{12}	Ω
Large Signal Voltage Gain	A_{VO}	$R_L = 2\text{ k}\Omega$, $V_O = -10\text{ V to }+10\text{ V}$	100	200		100	200		V/mV
		$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$	90	200		90	200		V/mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$				50	200		V/mV
OUTPUT CHARACTERISTICS									
Maximum Output Voltage Swing	$V_{O,MAX}$	$R_L = 10\text{ k}\Omega$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$	± 12	± 13.5		± 13	± 13.5		V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	± 12			± 13			V
		$R_L = 2\text{ k}\Omega$ $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$				± 13			V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$				± 12.5	± 13.3		V
Short-Circuit Output Current	I_{SC}		± 10			± 12			V
						± 12			V
				± 27			± 27		mA
POWER SUPPLY									
Power Supply Rejection Ratio	PSRR	$V_{DD} = 8\text{ V to }36\text{ V}$	80	86		80	86		dB
Supply Current per Amplifier	I_{SY}	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$		1.2	1.8		1.2	1.8	mA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			1.9			1.9	mA
								2.0	mA
DYNAMIC PERFORMANCE									
Slew Rate	SR			20			20		V/ μs
Gain Bandwidth Product	GBP			5			5		MHz
Phase Margin	ϕ_M			63			63		Degrees
Total Harmonic Distortion	THD	$V_{IN} = 6\text{ V rms}$, $f = 1\text{ kHz}$, $A_V = +1$, $R_L = 2\text{ k}\Omega$		0.001			0.001		%
Channel Separation	CS	$f = 10\text{ kHz}$		120			120		dB
NOISE PERFORMANCE									
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		16			16		nV/ $\sqrt{\text{Hz}}$

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	±18 V or +36 V
Input Voltage	±V supply
Differential Input Voltage	±V supply
Output Short Circuit to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature (Soldering 60 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC_N (R-8)	158	43	°C/W
8-Lead MSOP (RM-8)	210	45	°C/W
14-Lead SOIC_N (R-14)	120	36	°C/W
14-Lead TSSOP (RU-14)	180	35	°C/W

POWER SEQUENCING

The op amp supplies must be established simultaneously with, or before, any input signals are applied.

If this is not possible, the input current must be limited to 10 mA.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

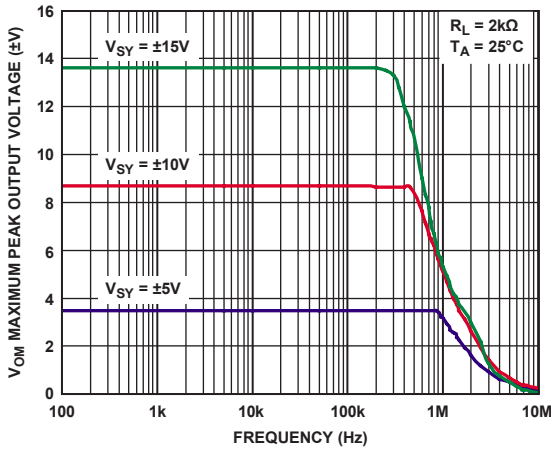


Figure 5. Maximum Peak Output Voltage vs. Frequency

06275-005

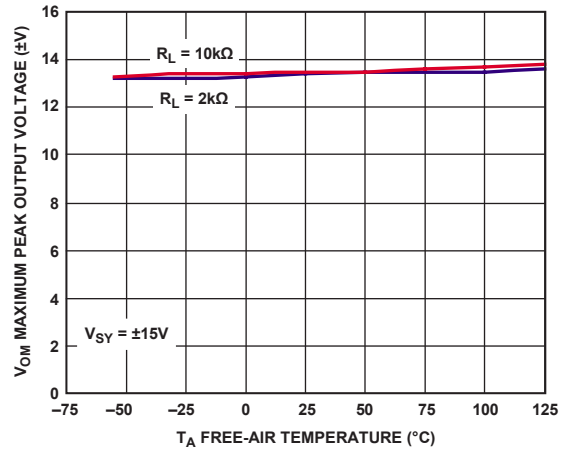


Figure 8. Maximum Peak Output Voltage vs. Free-Air Temperature

06275-008

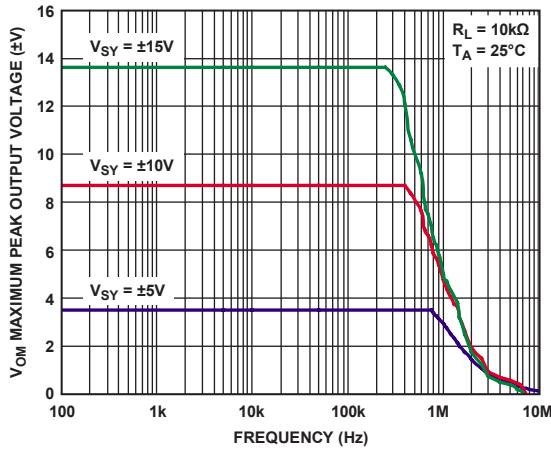


Figure 6. Maximum Peak Output Voltage vs. Frequency

06275-006

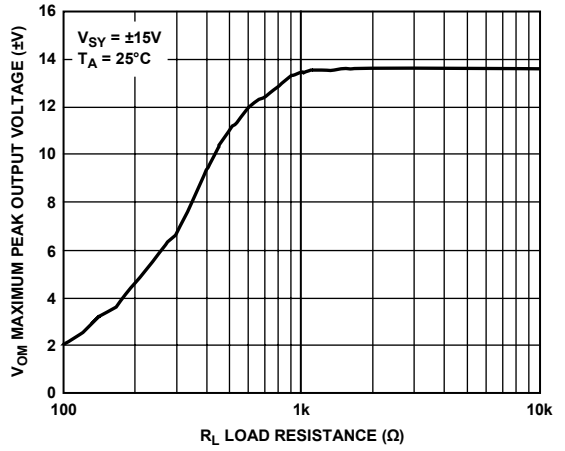


Figure 9. Maximum Peak Output Voltage vs. Load Resistance

06275-009

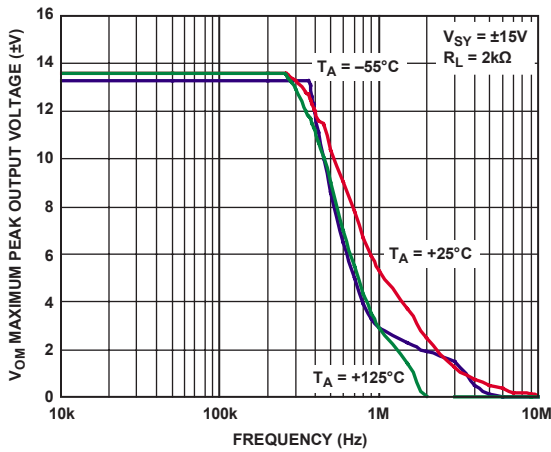


Figure 7. Maximum Peak Output Voltage vs. Frequency

06275-007

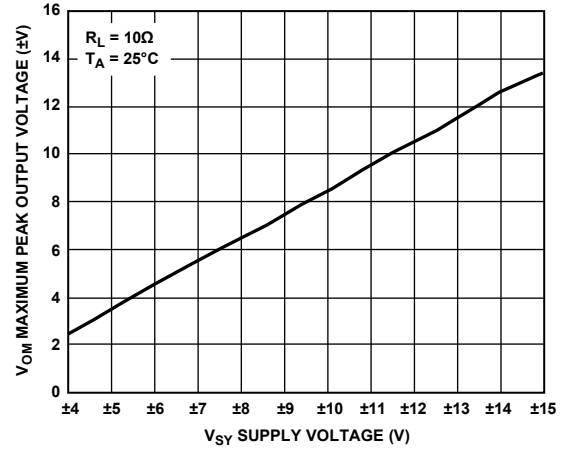


Figure 10. Maximum Peak Output Voltage vs. Supply Voltage

06275-010

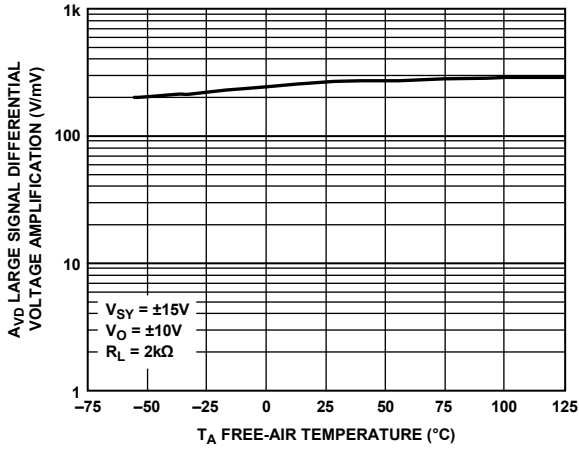


Figure 11. Large Signal Differential Voltage Amplification vs. Free-Air Temperature

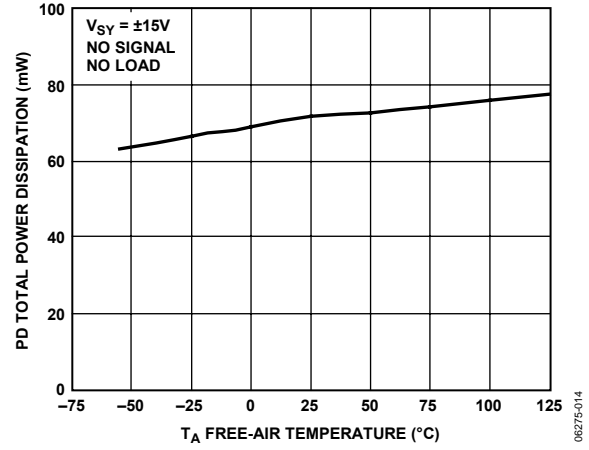


Figure 14. Total Power Dissipation vs. Free-Air Temperature

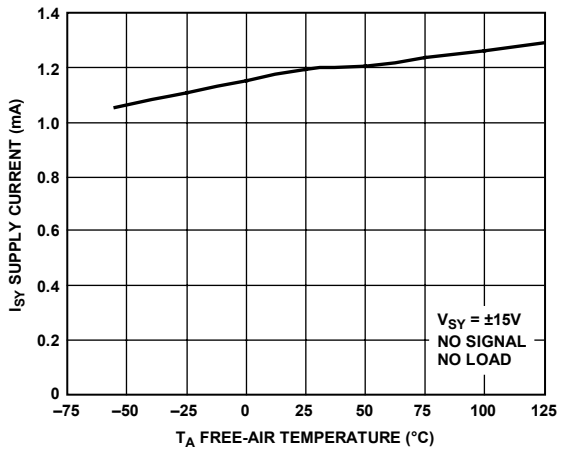


Figure 12. Supply Current Per Amplifier vs. Free-Air Temperature

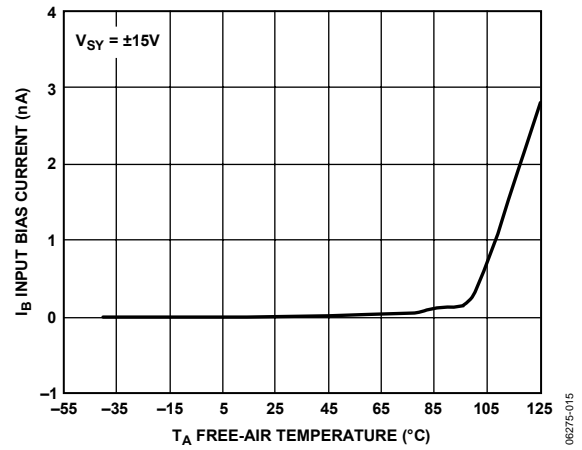


Figure 15. Input Bias Current vs. Free-Air Temperature

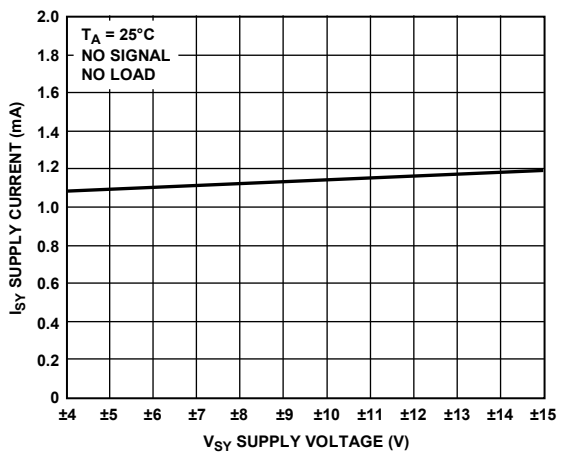


Figure 13. Supply Current vs. Supply Voltage

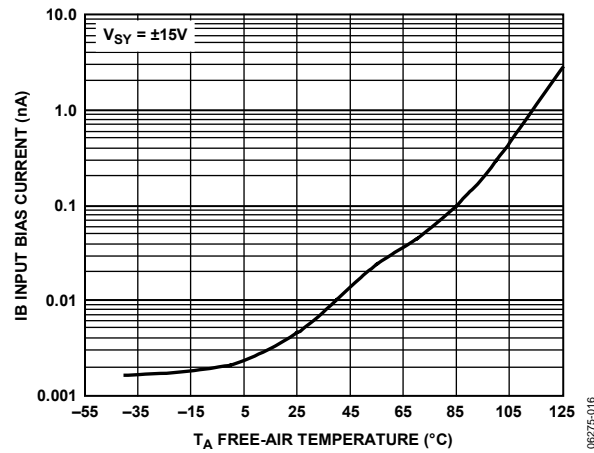


Figure 16. Input Bias Current vs. Free-Air Temperature

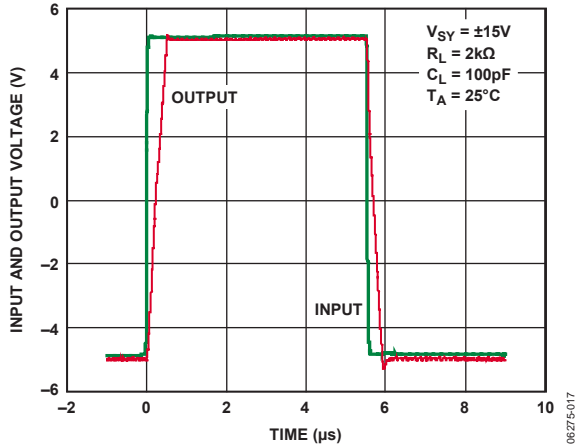


Figure 17. Large Signal Response

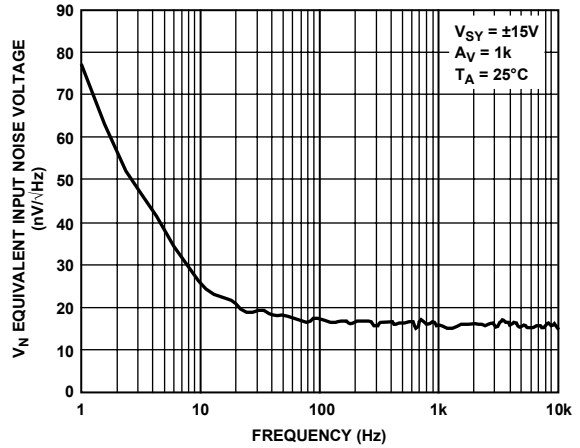


Figure 20. Voltage Noise Density vs. Frequency

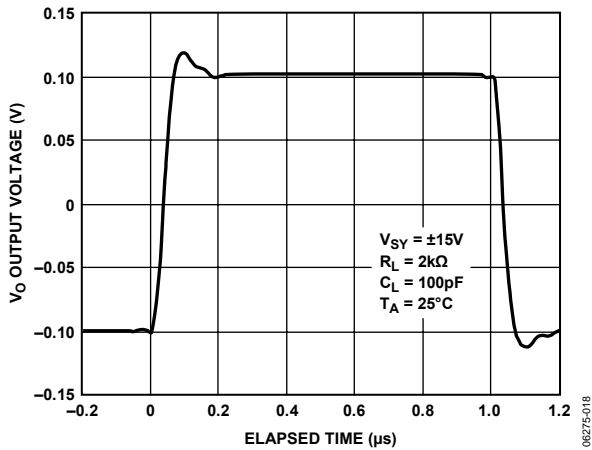


Figure 18. Small Signal Response

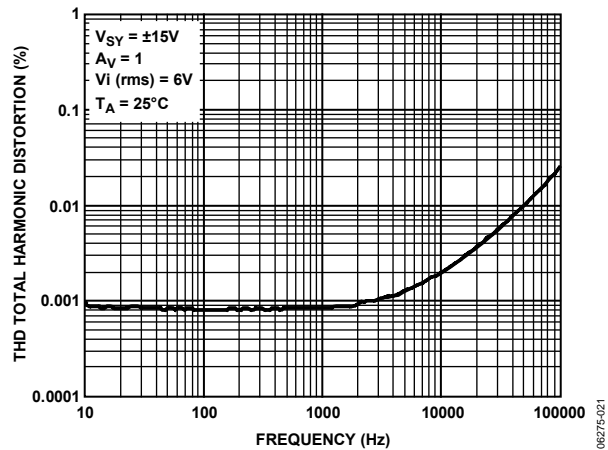


Figure 21. Total Harmonic Distortion vs. Frequency

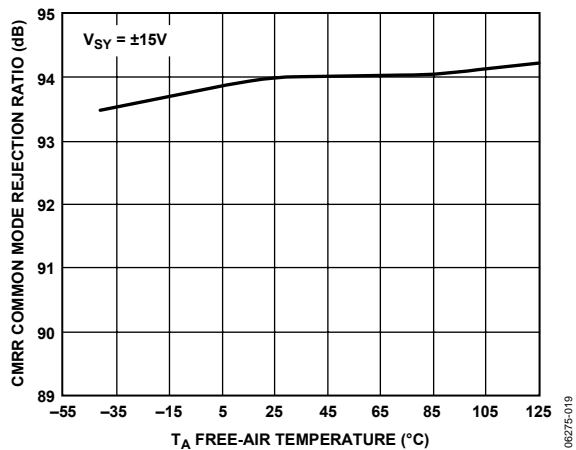
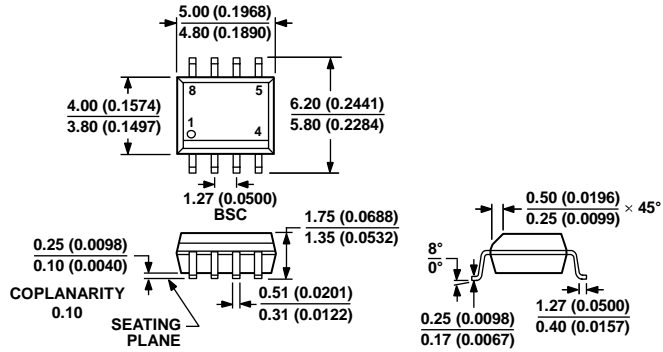


Figure 19. Common-Mode Rejection Ratio vs. Free-Air Temperature

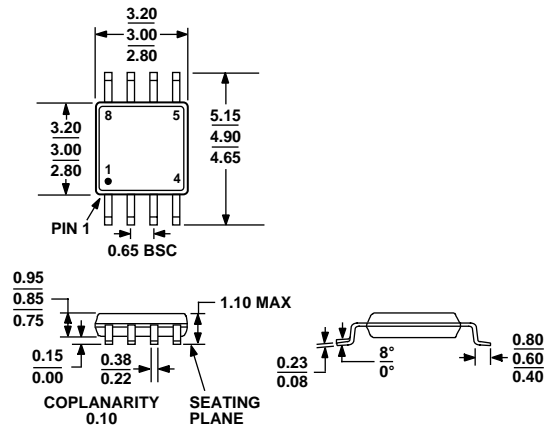
OUTLINE DIMENSIONS



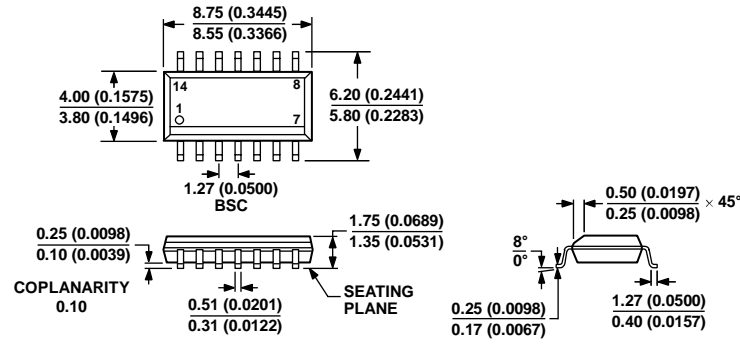
COMPLIANT TO JEDEC STANDARDS MS-012-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 22. 8-Lead Standard Small Outline Package [SOIC_N]
 Narrow Body (R-8)
 Dimensions shown in millimeters and (inches)

019407-A



COMPLIANT TO JEDEC STANDARDS MO-187-AA
 Figure 23. 8-Lead Mini Small Outline Package [MSOP]
 (RM-8)
 Dimensions shown in millimeters



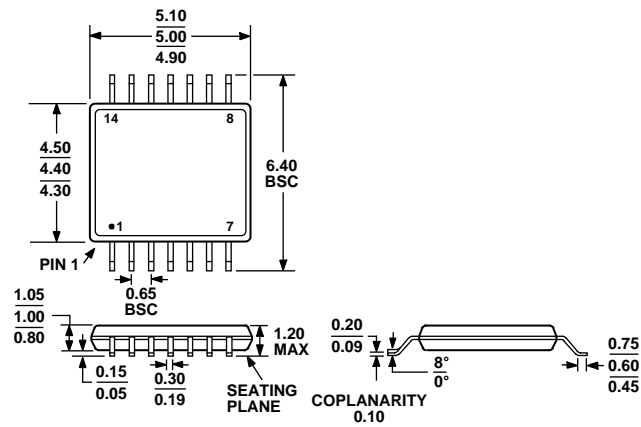
COMPLIANT TO JEDEC STANDARDS MS-012-AB
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 24. 14-Lead Standard Small Outline Package [SOIC_N]

Narrow Body (R-14)

Dimensions shown in millimeters and (inches)

060606-A



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 25. 14-Lead Thin Shrink Small Outline Package [TSSOP]
 (RU-14)

Dimensions shown in millimeters

ADTL082/ADTL084

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADTL082JR	0°C to +70°C	8-Lead SOIC_N	R-8	
ADTL082JR-REEL	0°C to +70°C	8-Lead SOIC_N	R-8	
ADTL082JR-REEL7	0°C to +70°C	8-Lead SOIC_N	R-8	
ADTL082JRZ ¹	0°C to +70°C	8-Lead SOIC_N	R-8	
ADTL082JRZ-REEL ¹	0°C to +70°C	8-Lead SOIC_N	R-8	
ADTL082JRZ-REEL7 ¹	0°C to +70°C	8-Lead SOIC_N	R-8	
ADTL082ARZ ¹	-40°C to +125°C	8-Lead SOIC_N	R-8	
ADTL082ARZ-REEL ¹	-40°C to +125°C	8-Lead SOIC_N	R-8	
ADTL082ARZ-REEL7 ¹	-40°C to +125°C	8-Lead SOIC_N	R-8	
ADTL082ARMZ-R2 ¹	-40°C to +125°C	8-Lead MSOP	RM-8	A18
ADTL082ARMZ-REEL ¹	-40°C to +125°C	8-Lead MSOP	RM-8	A18
ADTL084JR	0°C to +70°C	14-Lead SOIC_N	R-14	
ADTL084JR-REEL	0°C to +70°C	14-Lead SOIC_N	R-14	
ADTL084JR-REEL7	0°C to +70°C	14-Lead SOIC_N	R-14	
ADTL084JRZ ¹	0°C to +70°C	14-Lead SOIC_N	R-14	
ADTL084JRZ-REEL ¹	0°C to +70°C	14-Lead SOIC_N	R-14	
ADTL084JRZ-REEL7 ¹	0°C to +70°C	14-Lead SOIC_N	R-14	
ADTL084ARZ ¹	-40°C to +125°C	14-Lead SOIC_N	R-14	
ADTL084ARZ-REEL ¹	-40°C to +125°C	14-Lead SOIC_N	R-14	
ADTL084ARZ-REEL7 ¹	-40°C to +125°C	14-Lead SOIC_N	R-14	
ADTL084ARUZ ¹	-40°C to +125°C	14-lead TSSOP	RU-14	
ADTL084ARUZ-REEL ¹	-40°C to +125°C	14-lead TSSOP	RU-14	

¹ Z = RoHS Compliant Part.

NOTES

NOTES